

Fig.1

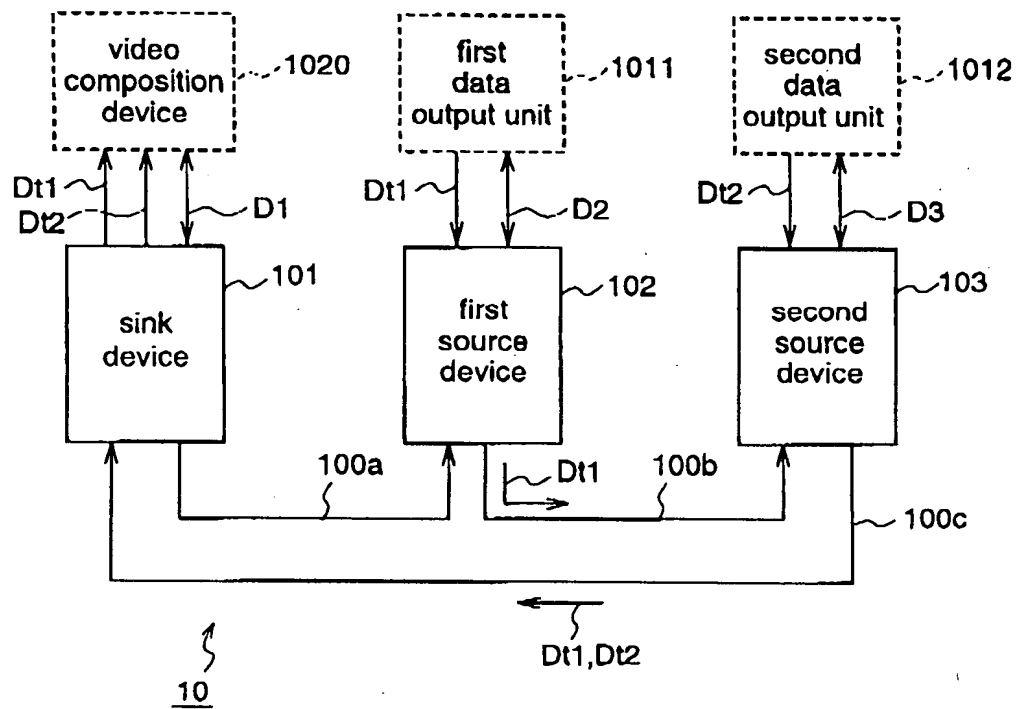


Fig.2 (b)

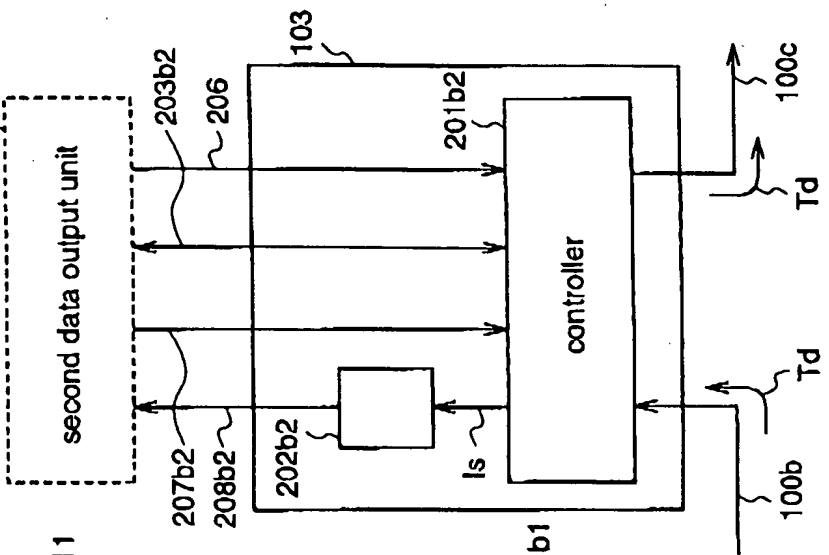
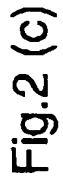


Fig.3

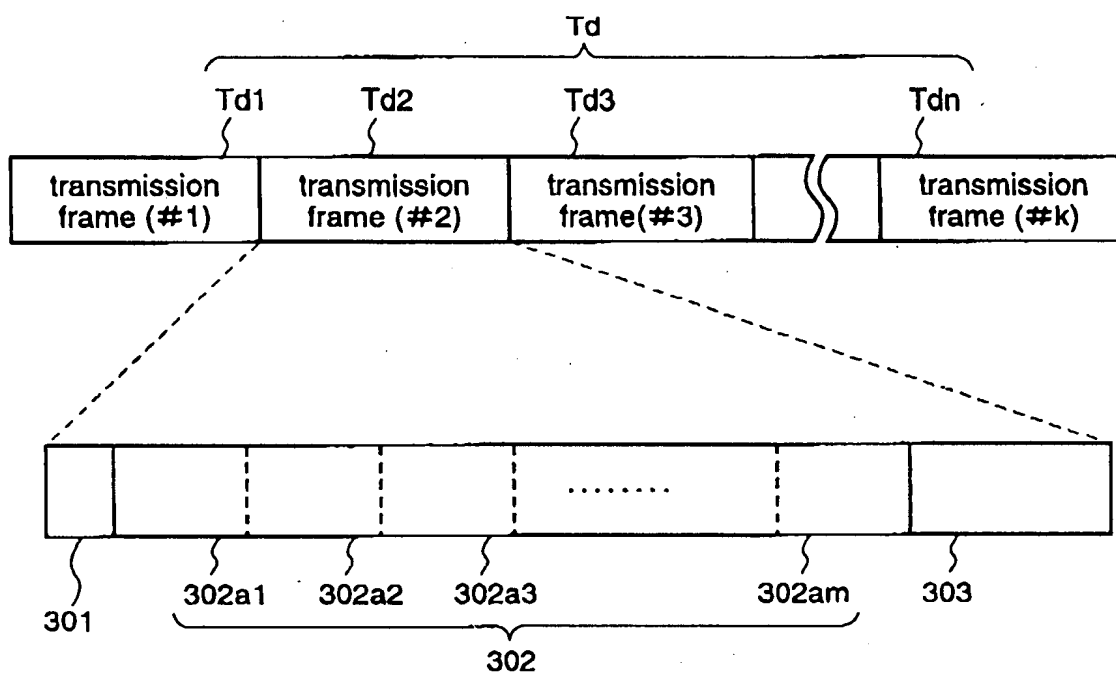


Fig.4 (a)

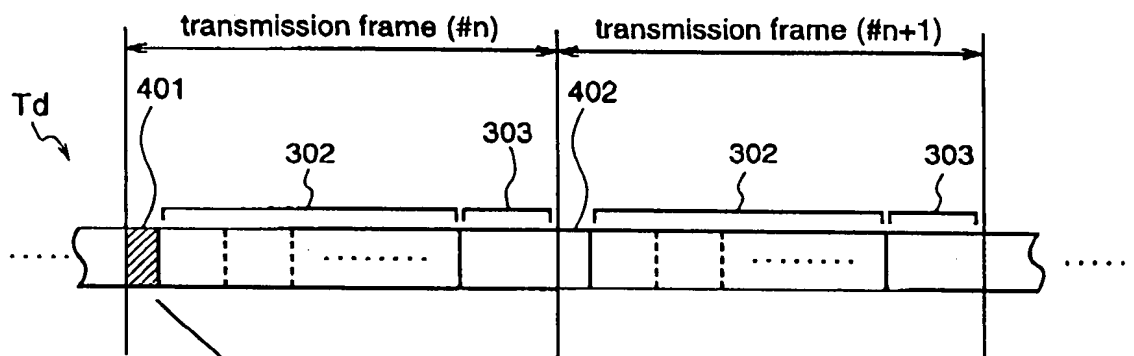
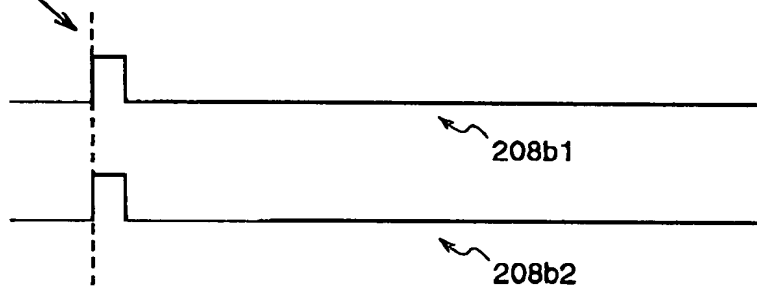
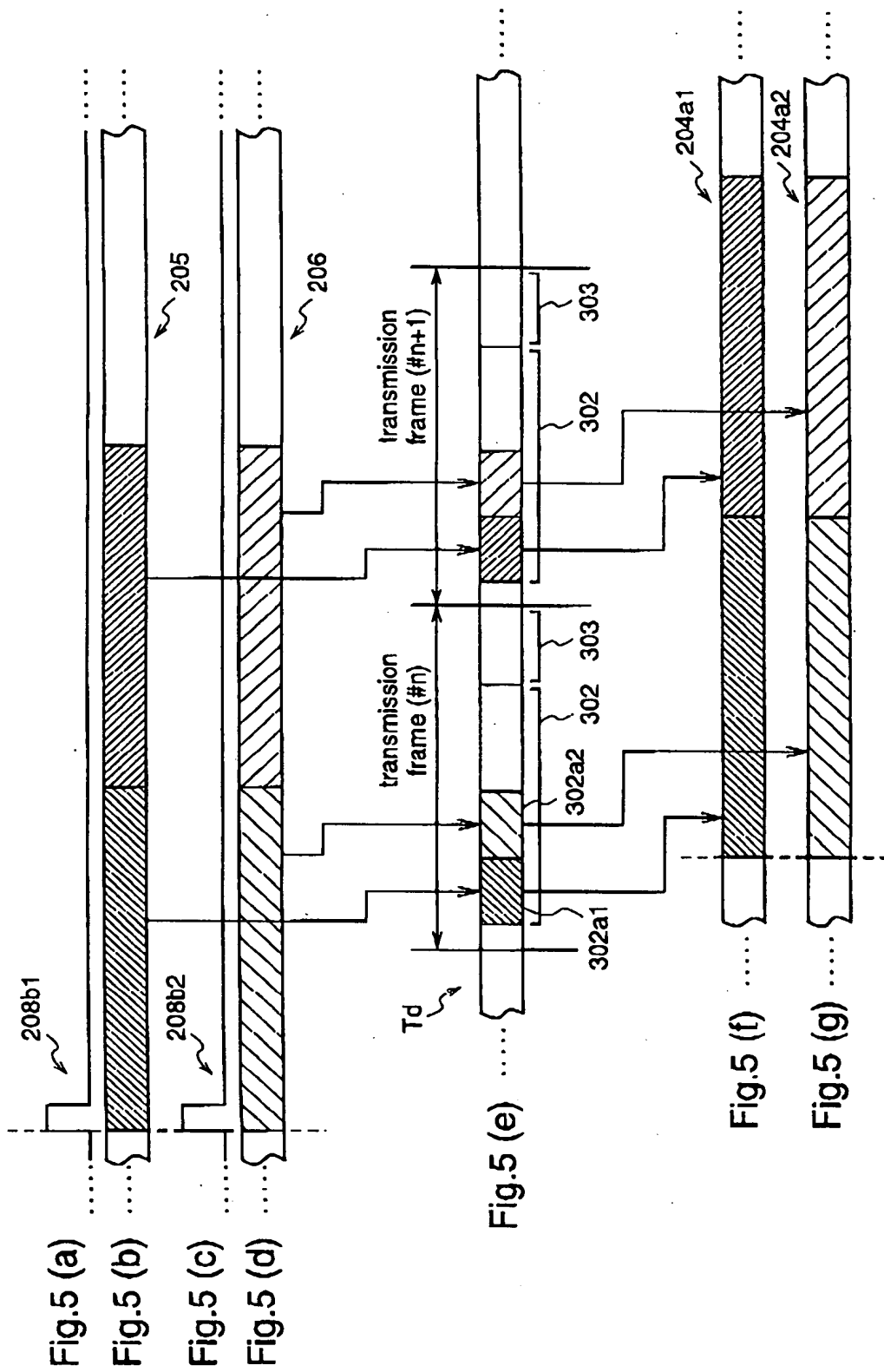


Fig.4 (b)

Fig.4 (c)





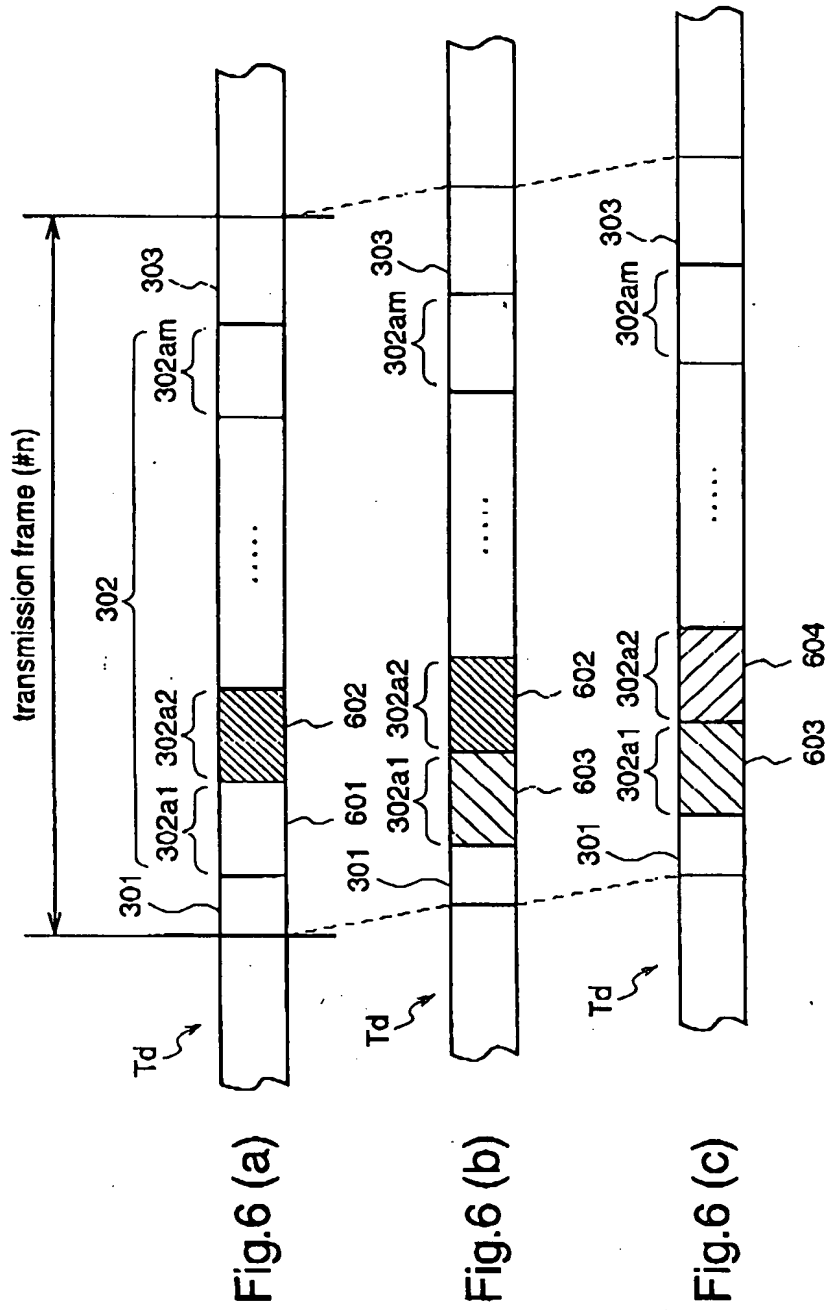


Fig.7

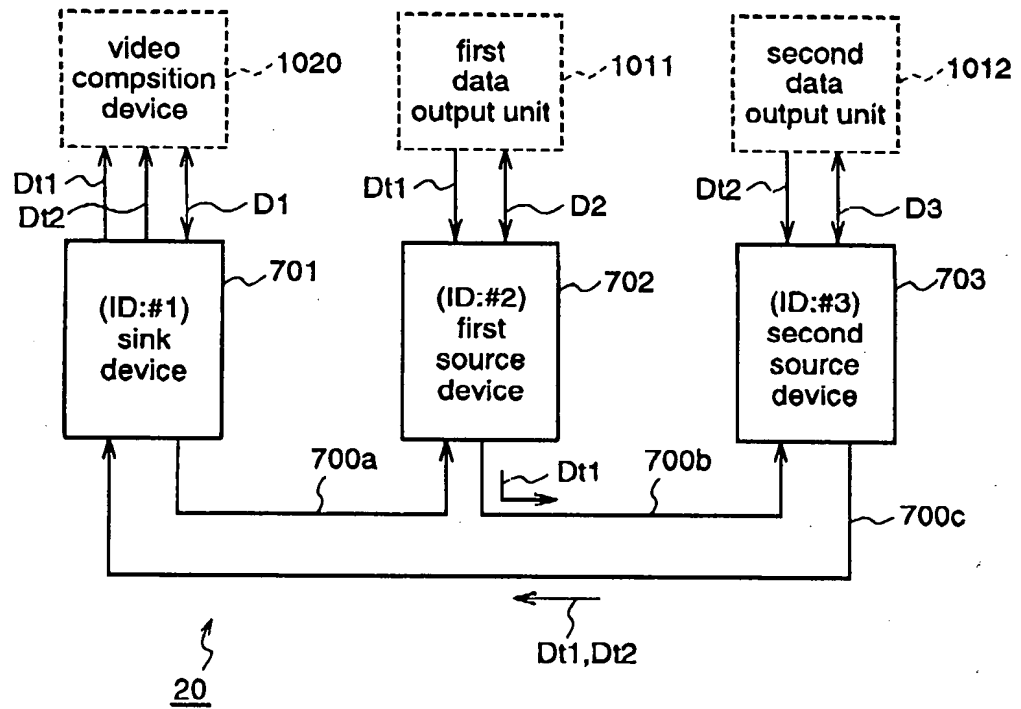


Fig.8 (a)

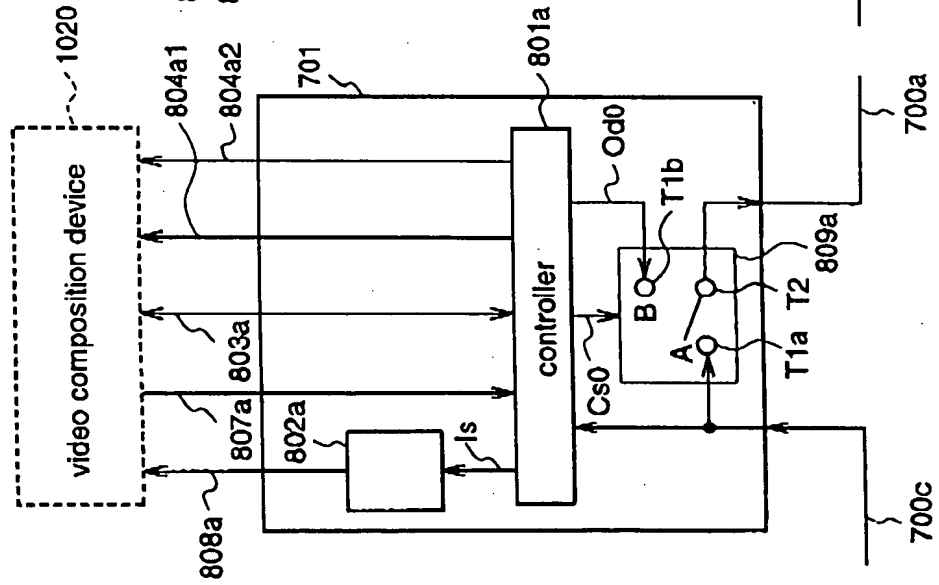


Fig.8 (b)

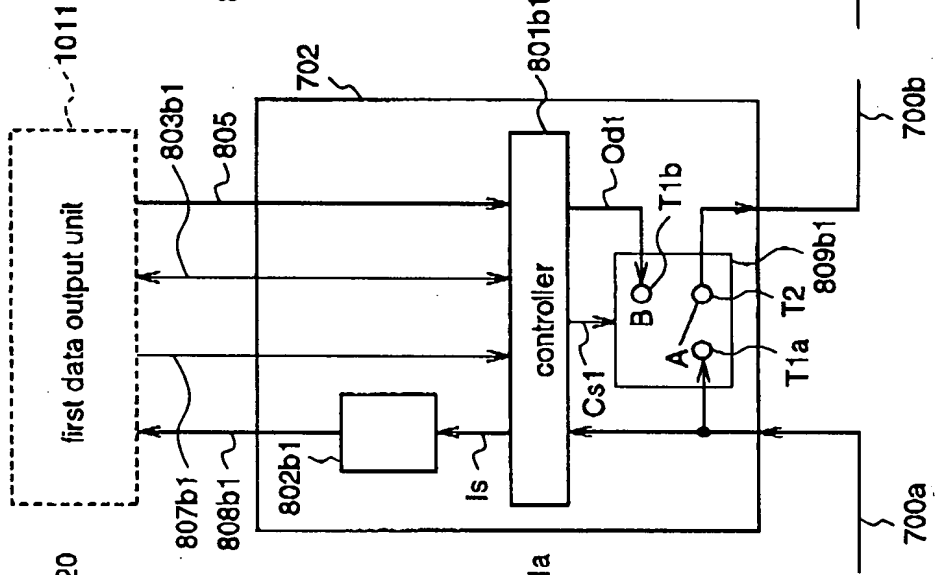


Fig.8 (c)

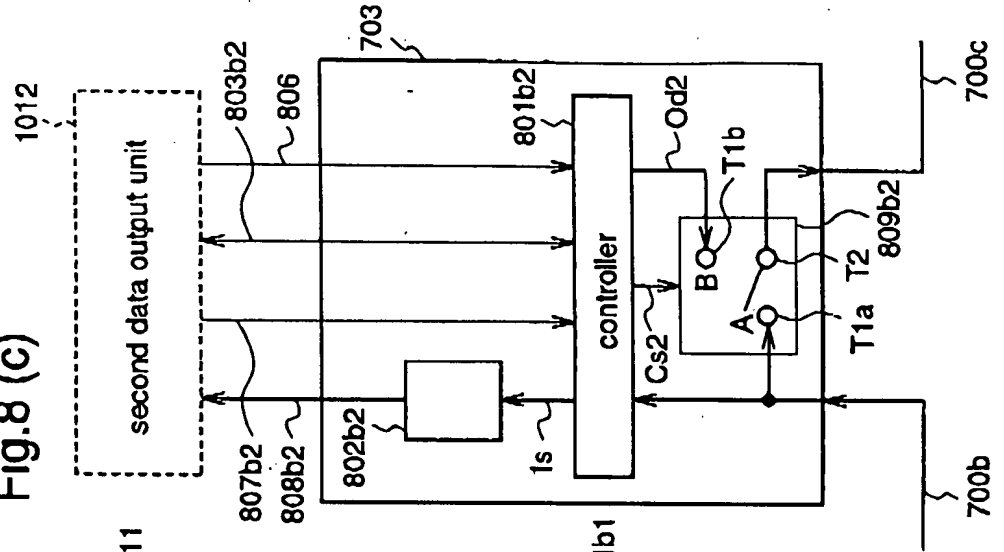


Fig.9

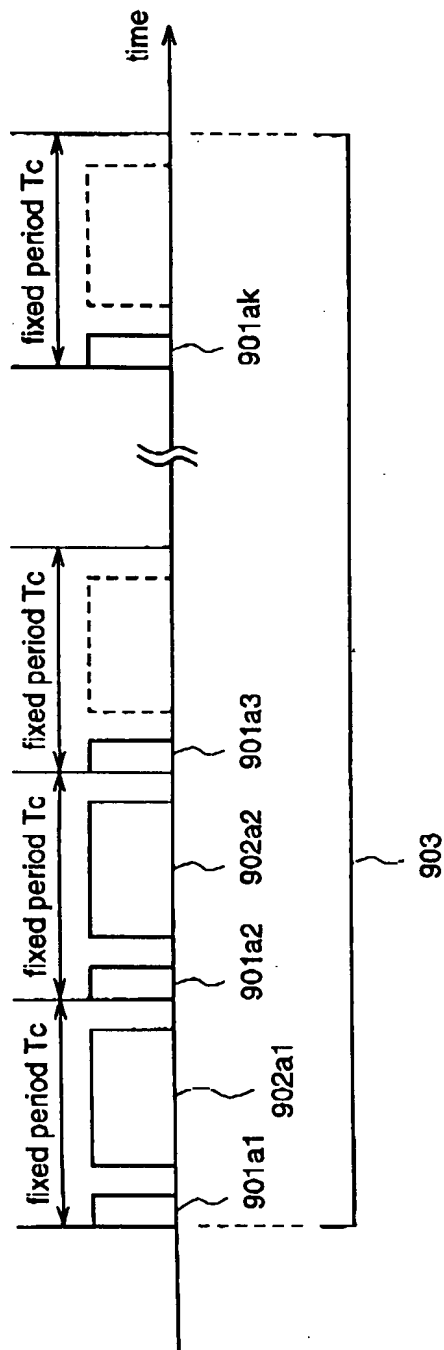


Fig.10 (a)

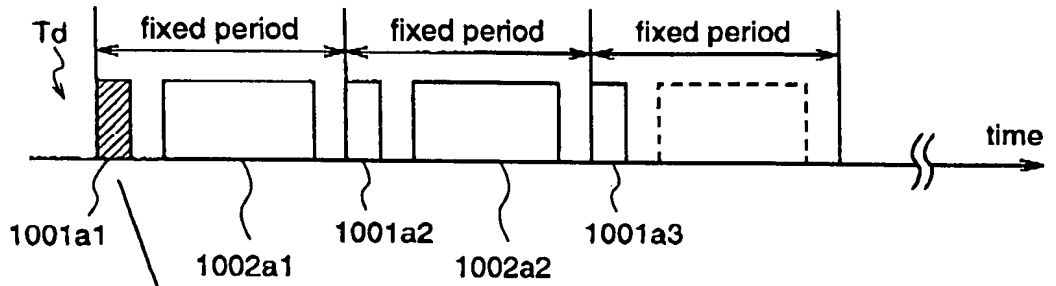
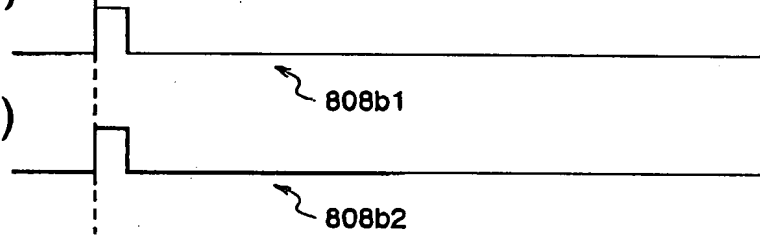


Fig.10 (b)

Fig.10 (c)



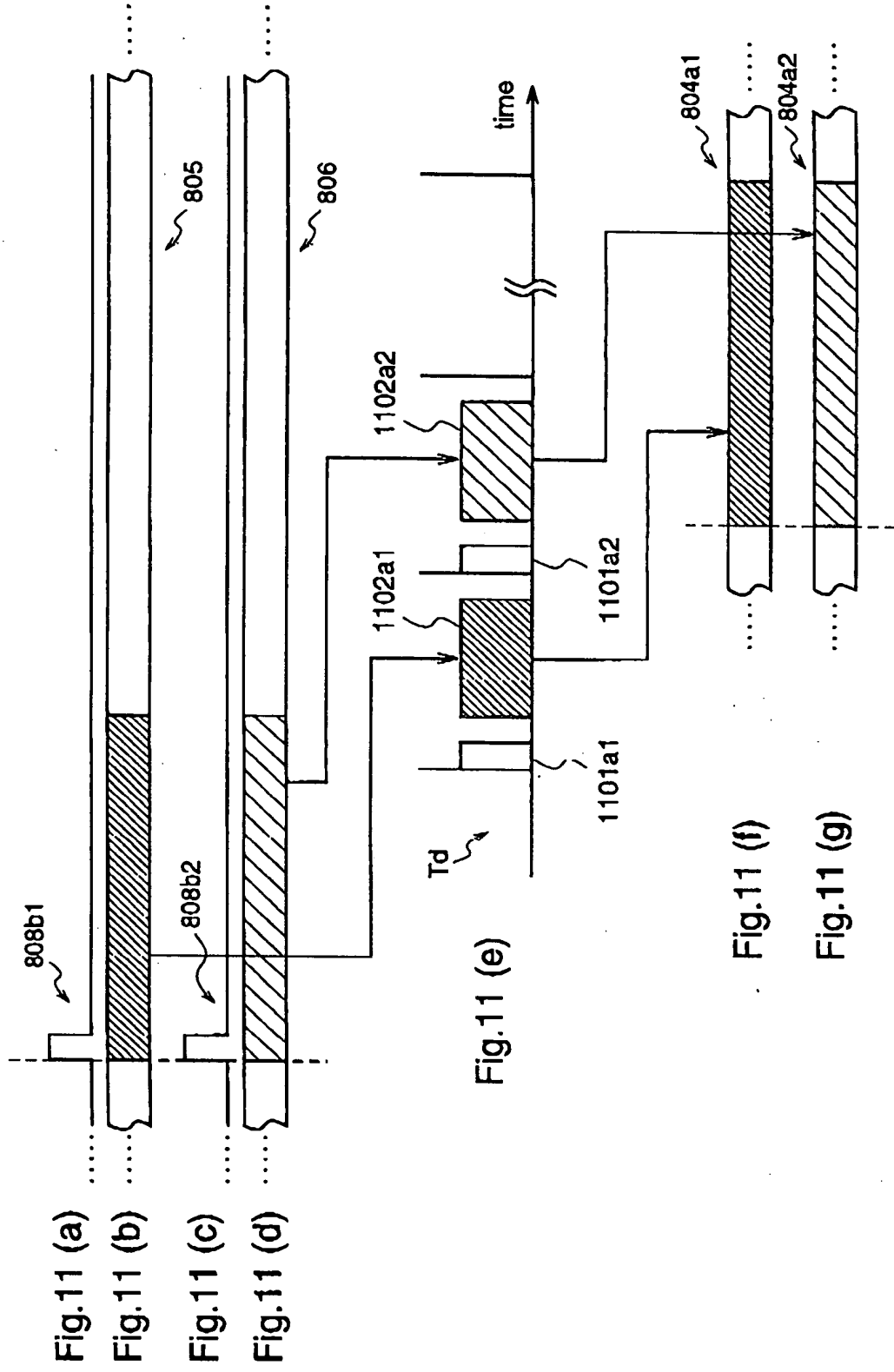


Fig.12

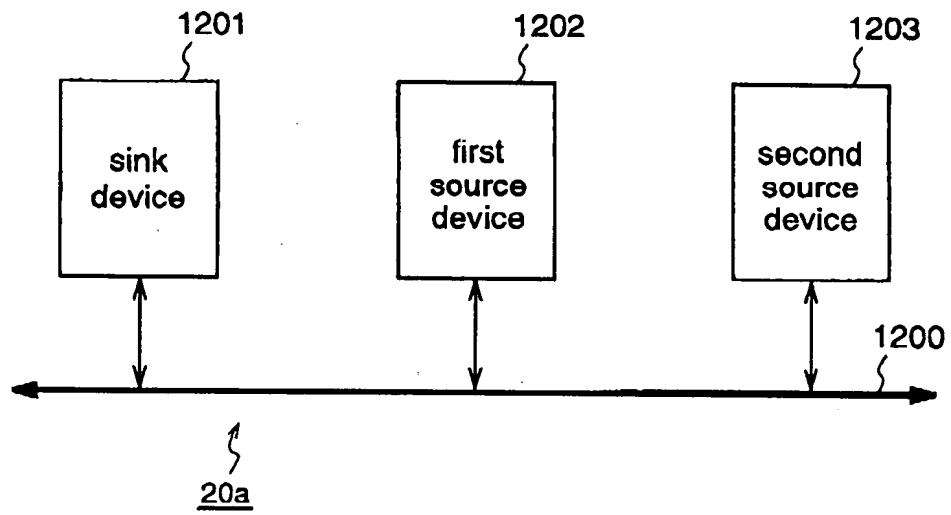


Fig.13

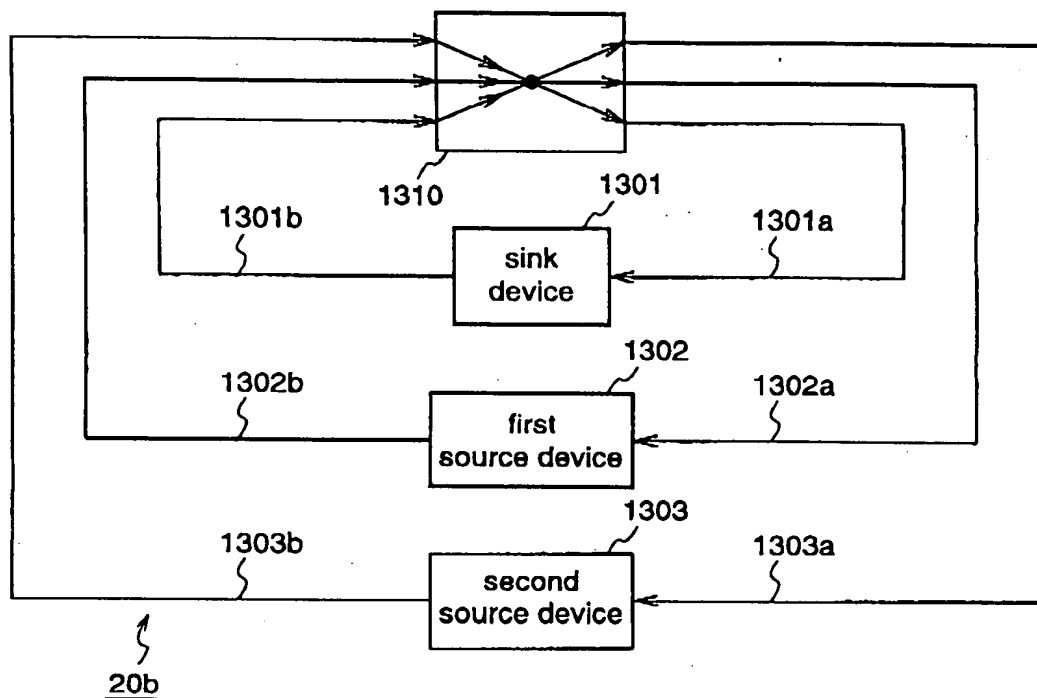


Fig.14

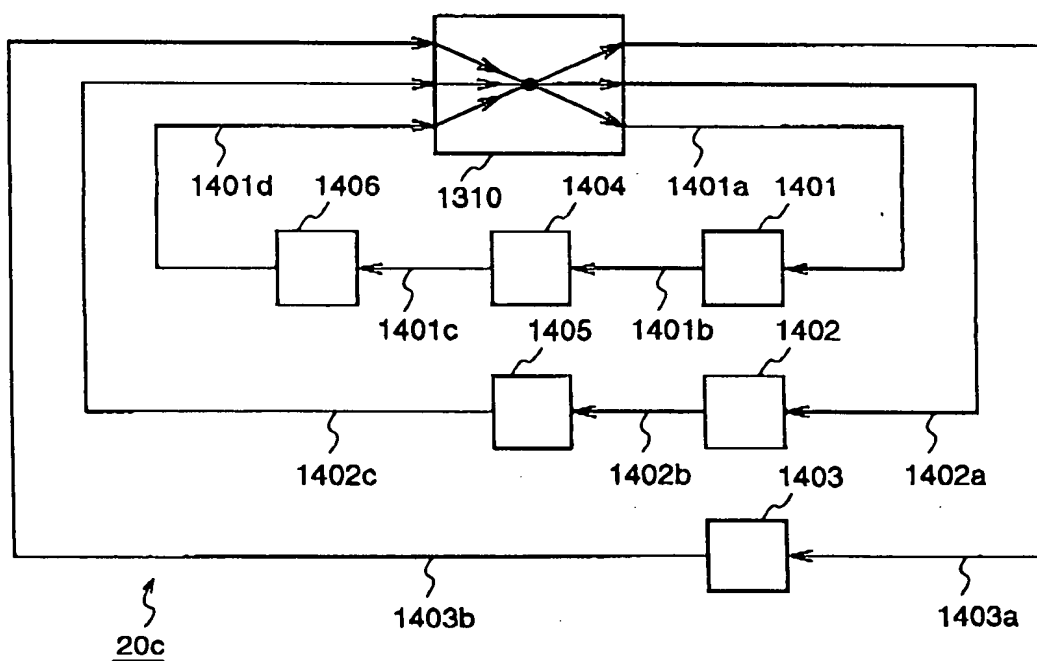


Fig.15

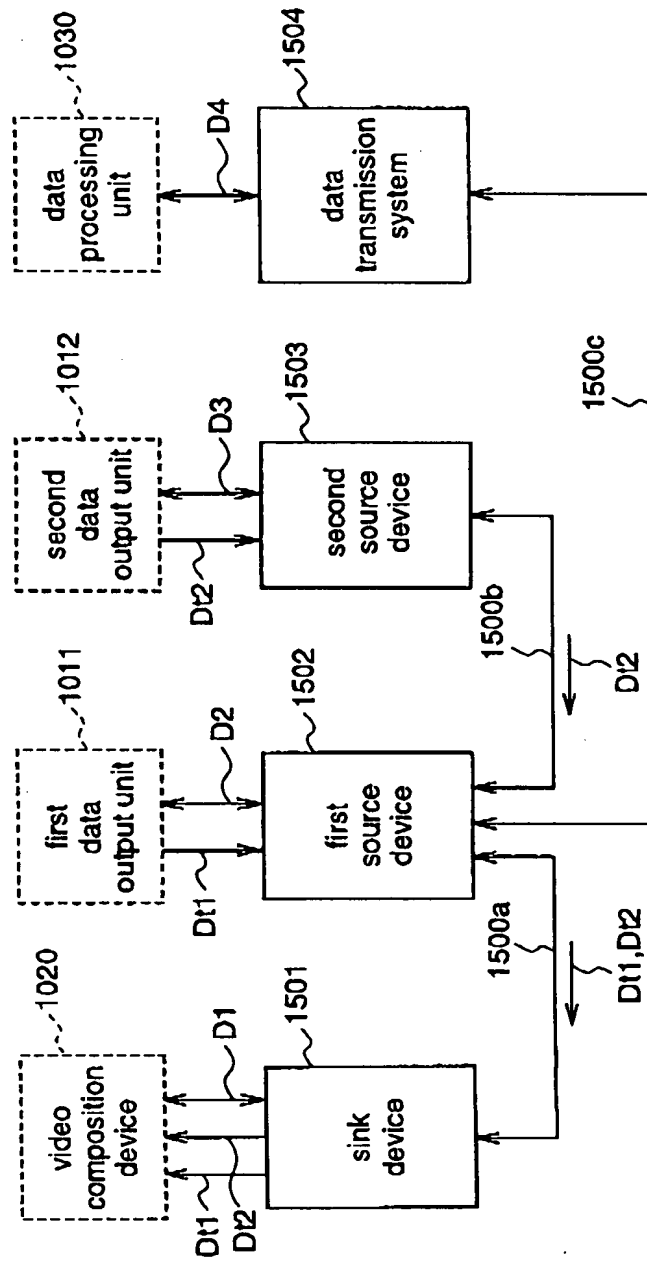


Fig.16 (a)

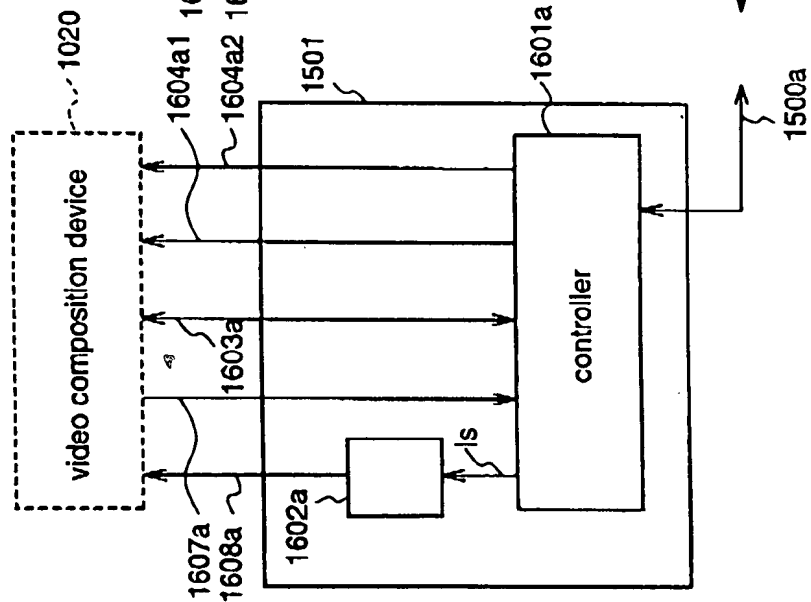


Fig.16 (b)

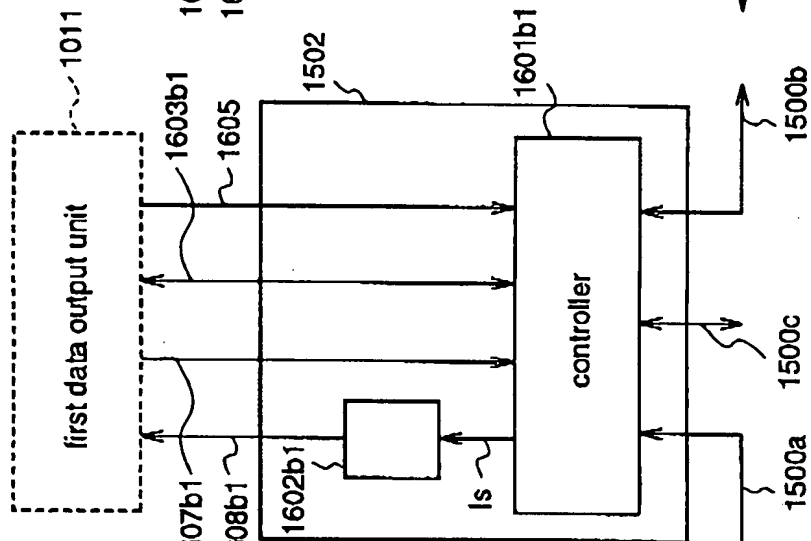


Fig.16 (c)

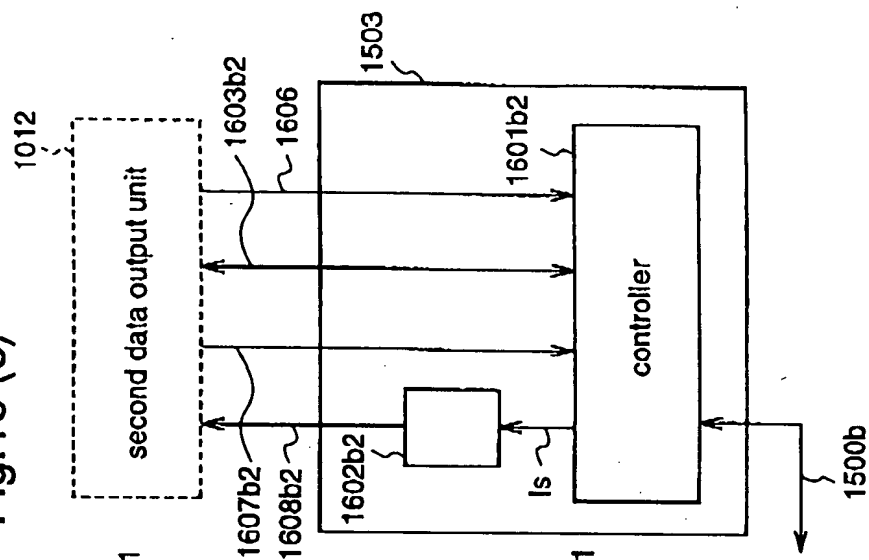
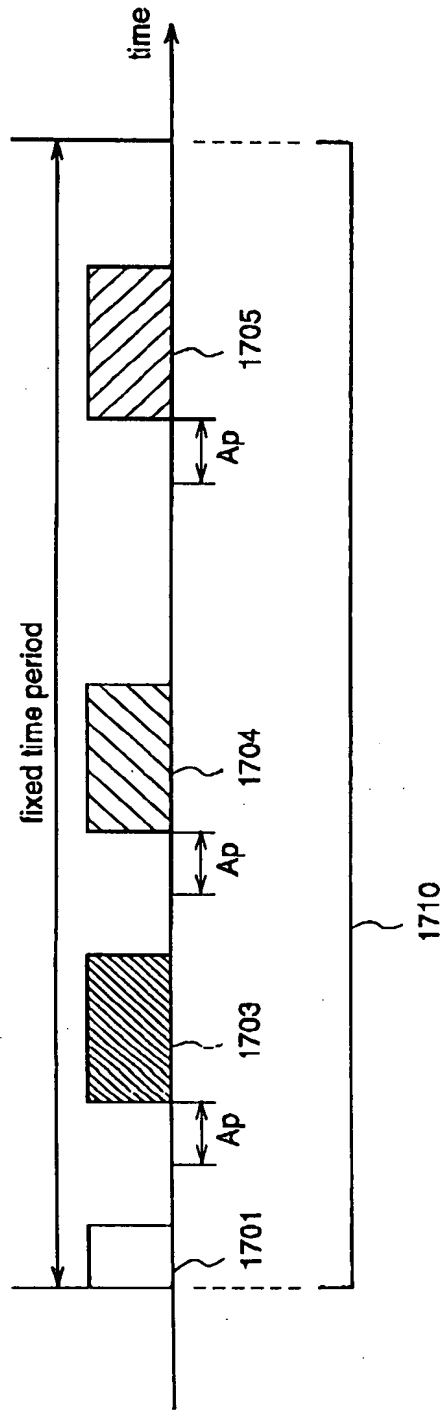
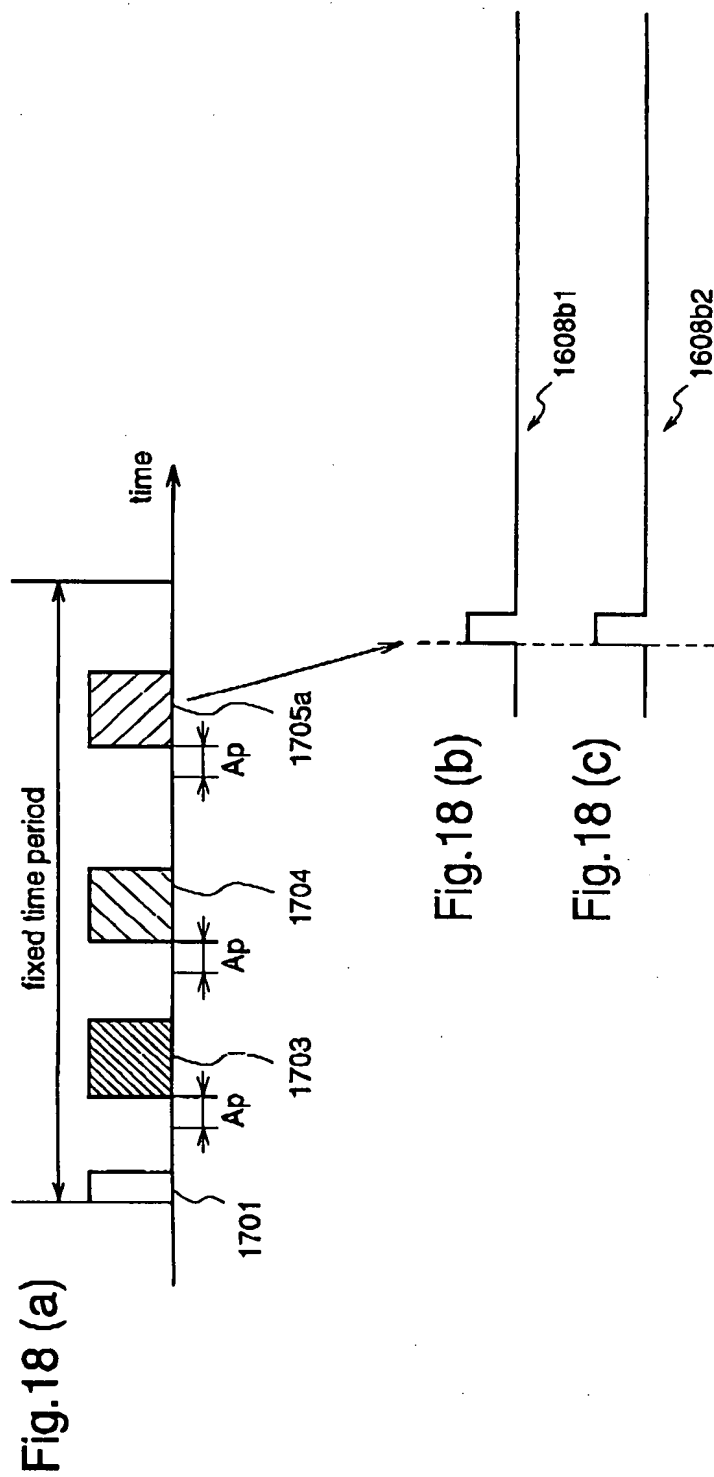


Fig.17





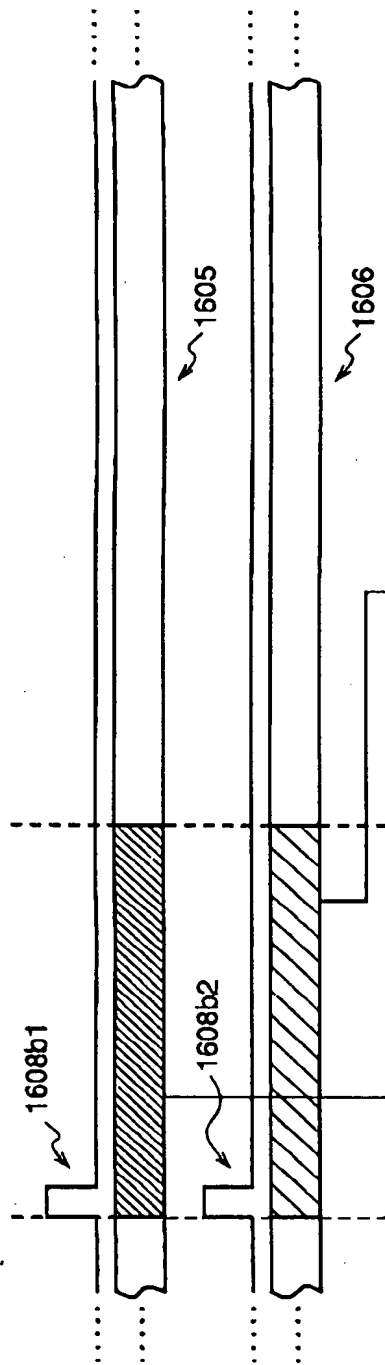


Fig. 19 (a)

Fig. 19 (b)

Fig. 19 (c)

Fig. 19 (d)

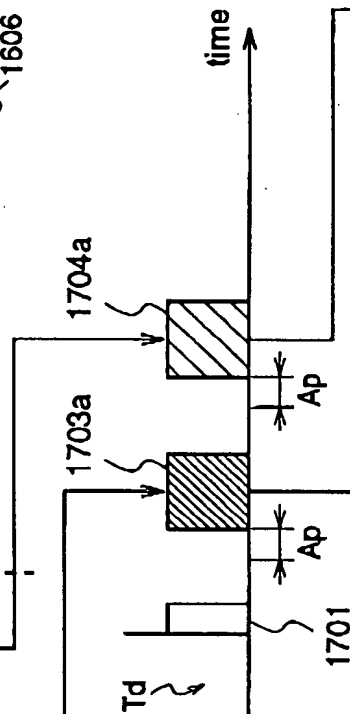


Fig. 19 (e)

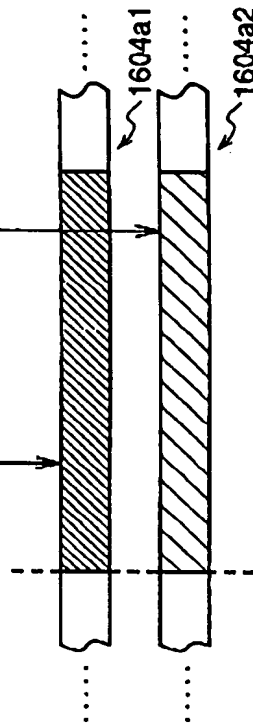


Fig. 19 (f)

Fig. 19 (g)

Fig.20

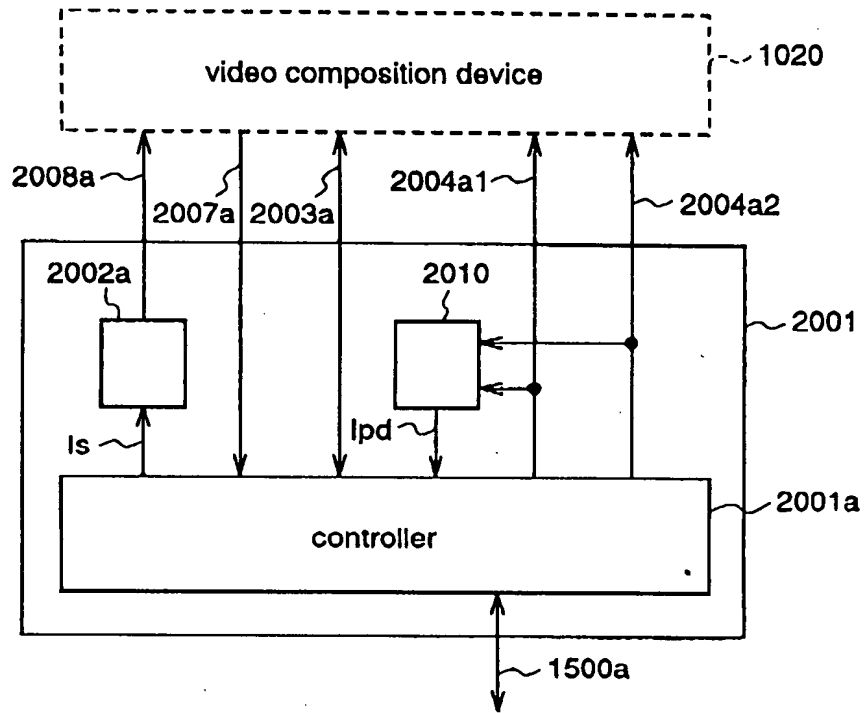


FIG. 21 is a schematic diagram of a device 1600 in a first state. The device 1600 includes a substrate 1606 and a layer 1608a. The layer 1608a is divided into a first portion 1608a1 and a second portion 1608a2. The first portion 1608a1 is a solid layer, and the second portion 1608a2 is a hatched layer. The thickness of the first portion 1608a1 is indicated by a dimension line and the label Pd. The device 1600 is shown in a first state, where the first portion 1608a1 is in contact with the substrate 1606.

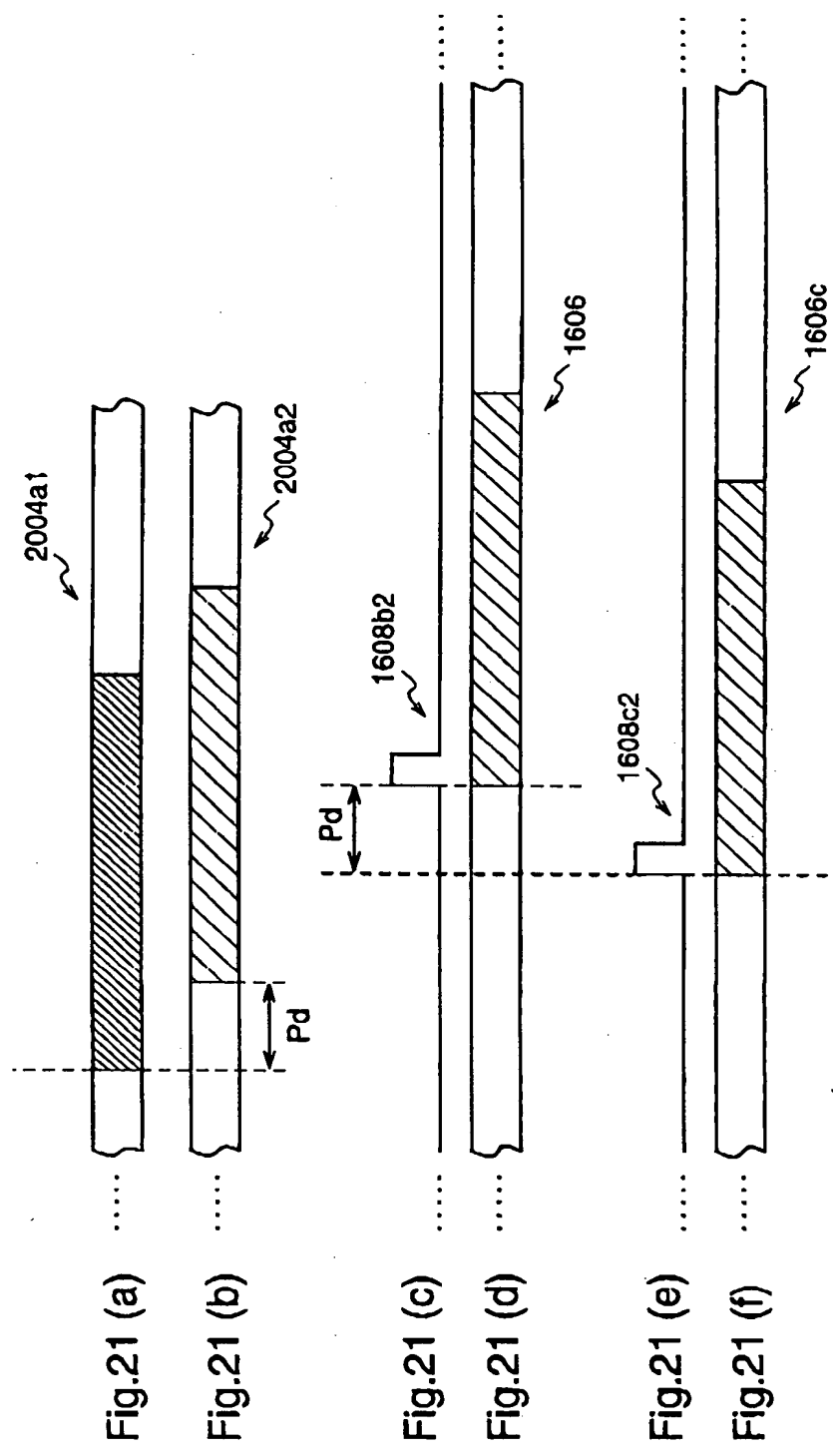


Fig.22

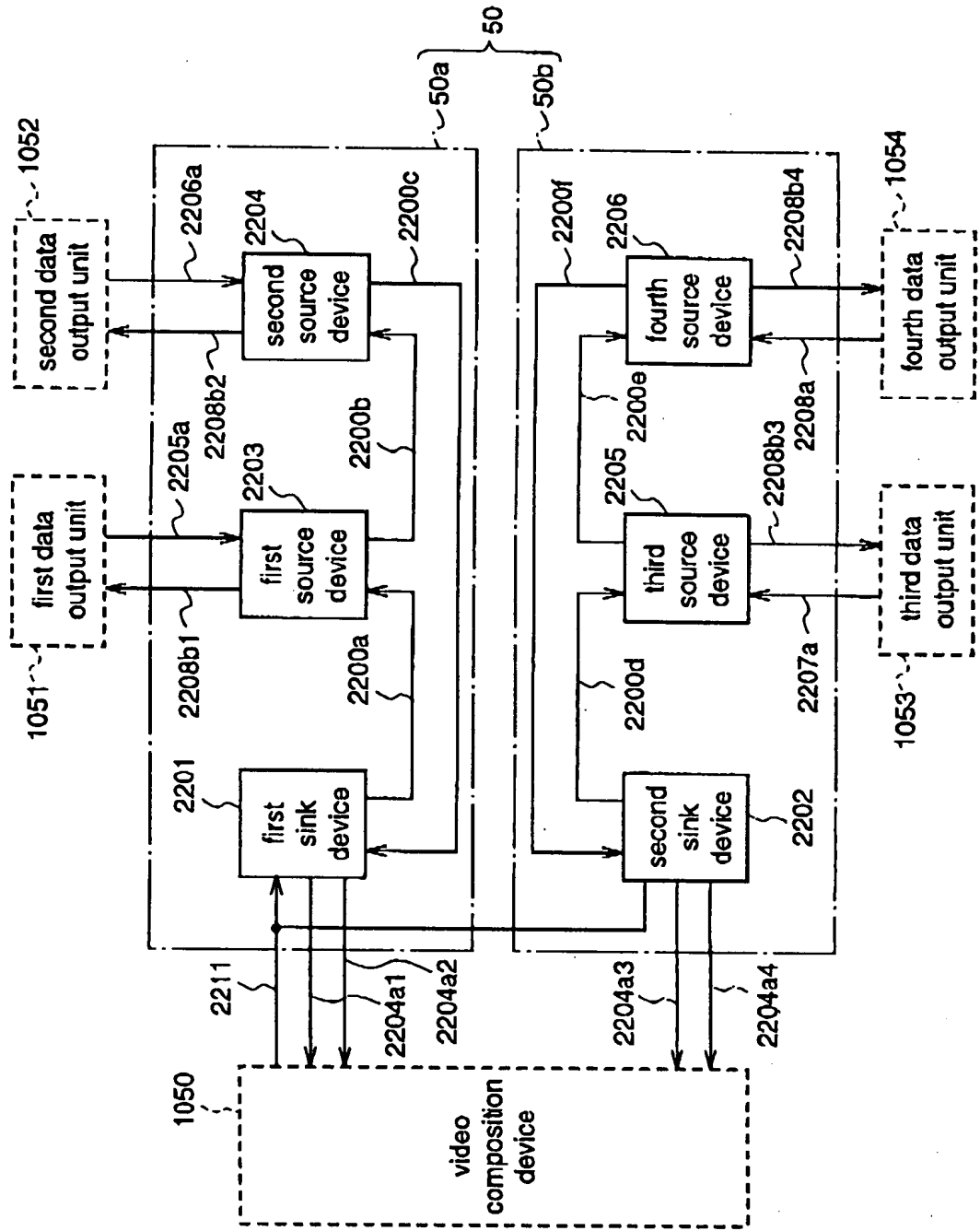


Fig.23

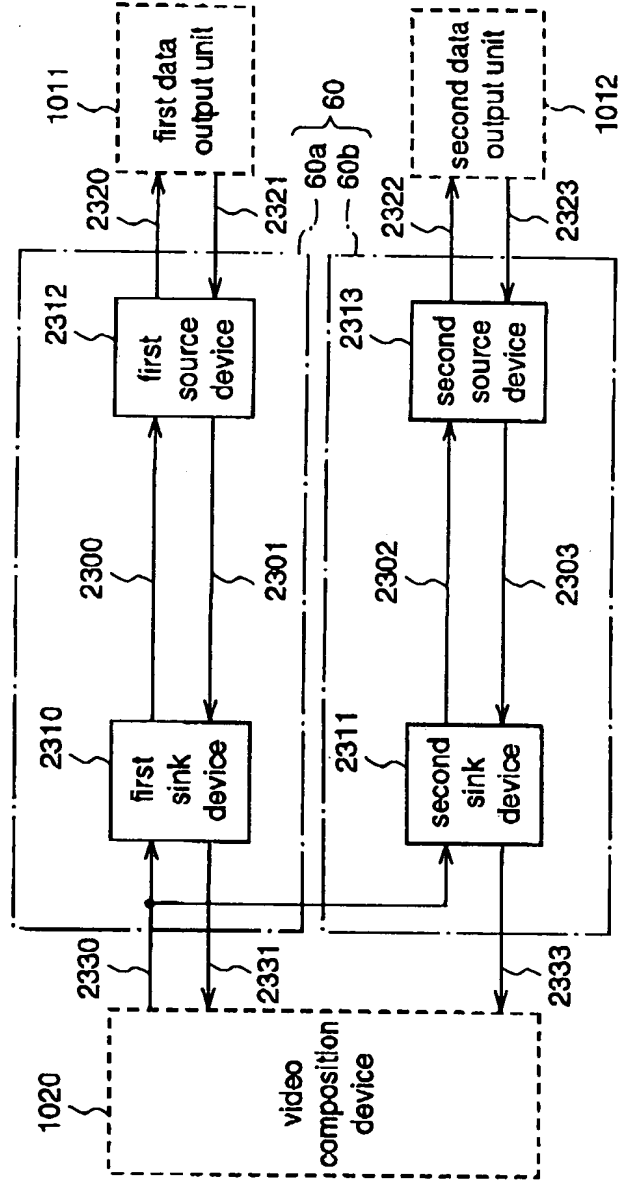


Fig.24 (a)

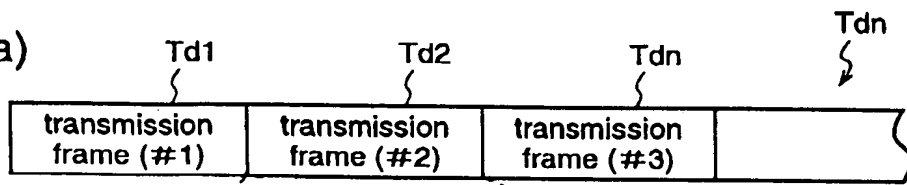


Fig.24 (b)

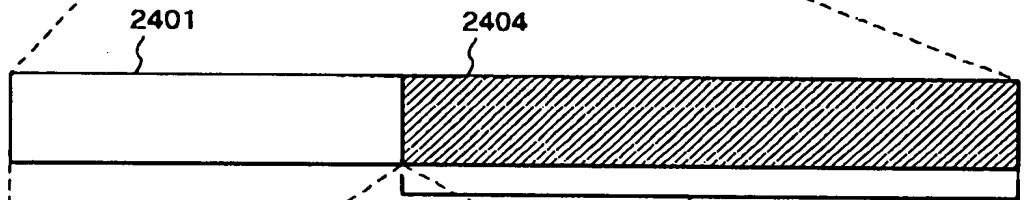


Fig.24 (c)

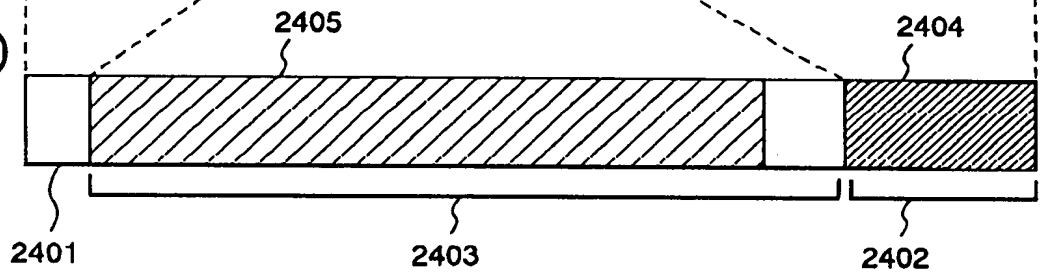
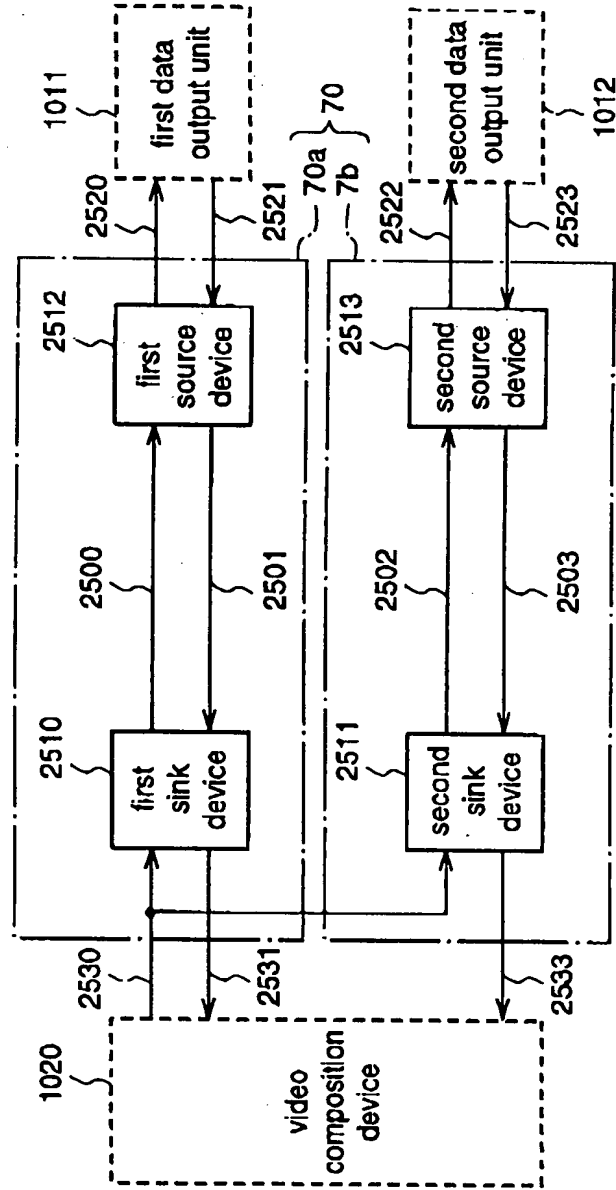


Fig.25



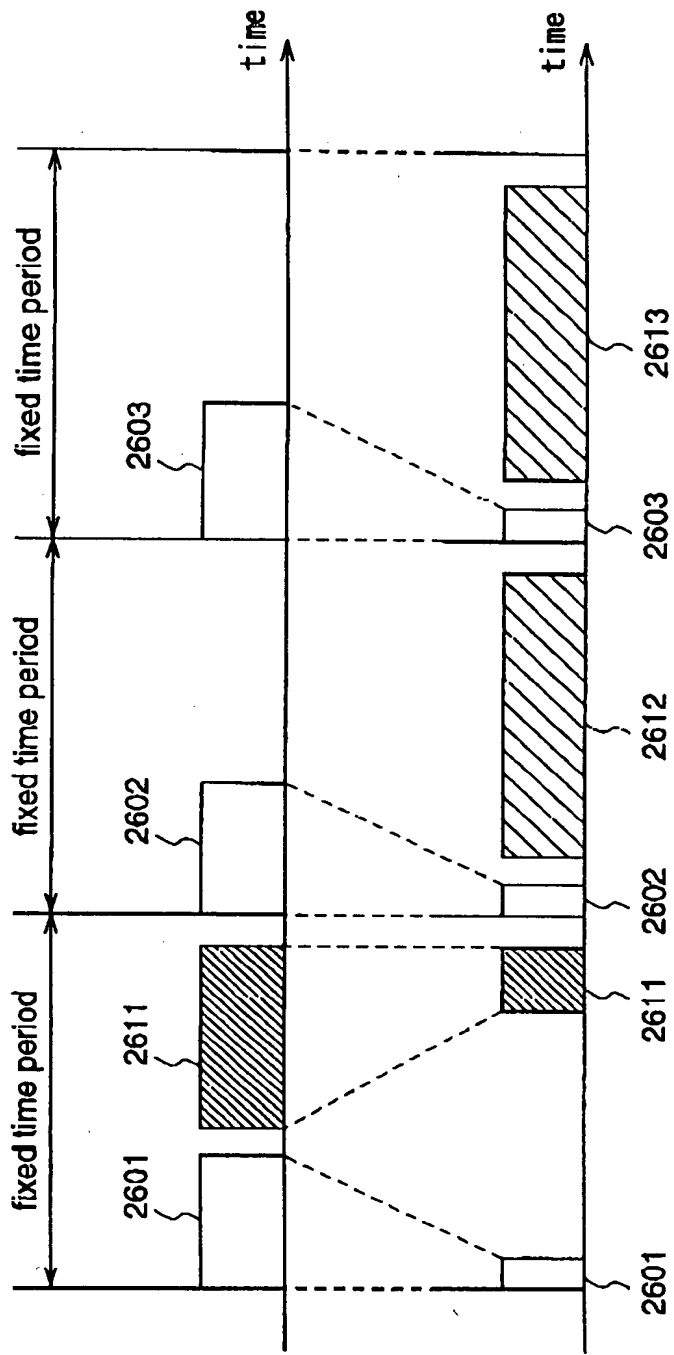


Fig.26 (a)

Fig.26 (b)

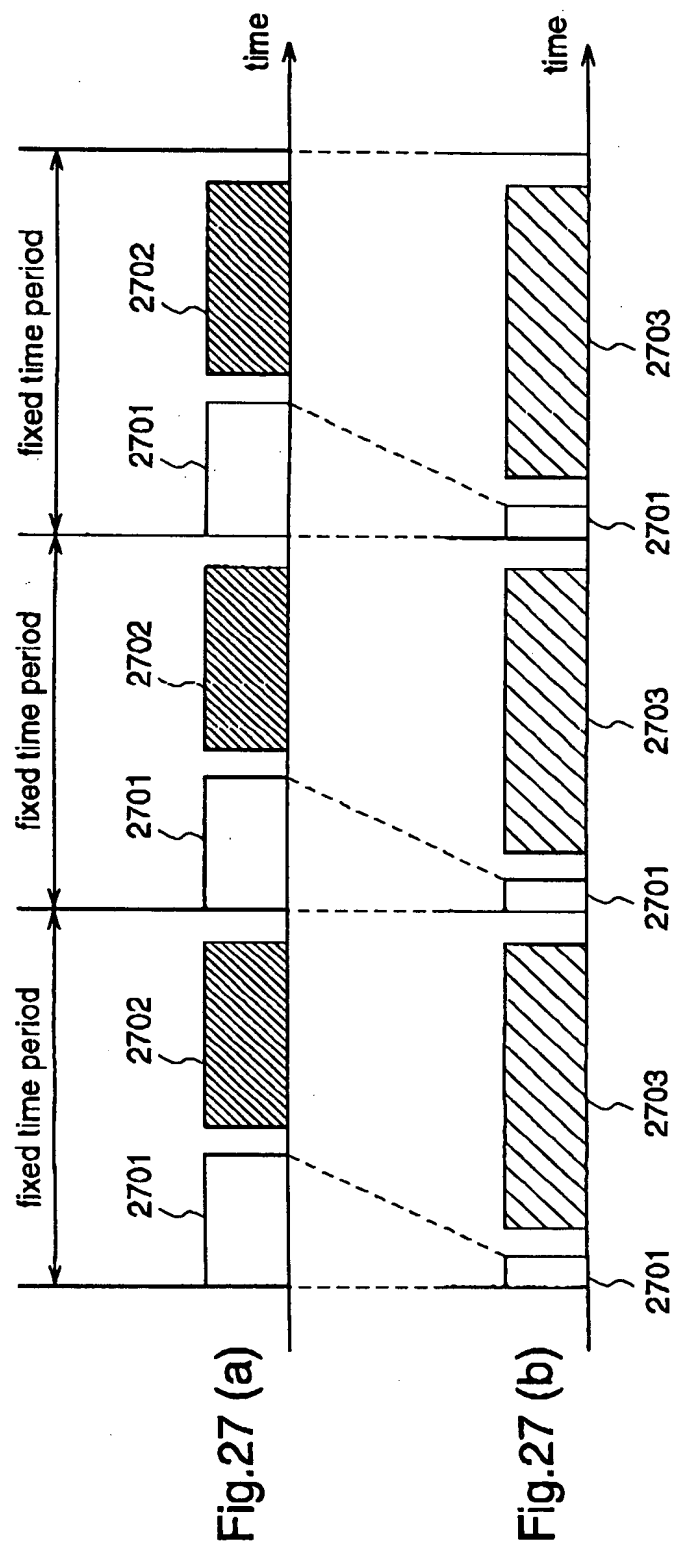


FIG. 28 is a schematic diagram of a semiconductor device in a cross-sectional view. The device includes a substrate 2801, a gate stack 2802, a channel layer 2803, and a source/drain layer 2804. A dashed line 2805 indicates the position of the channel layer. The device is shown in a cross-sectional view along a line A-A.

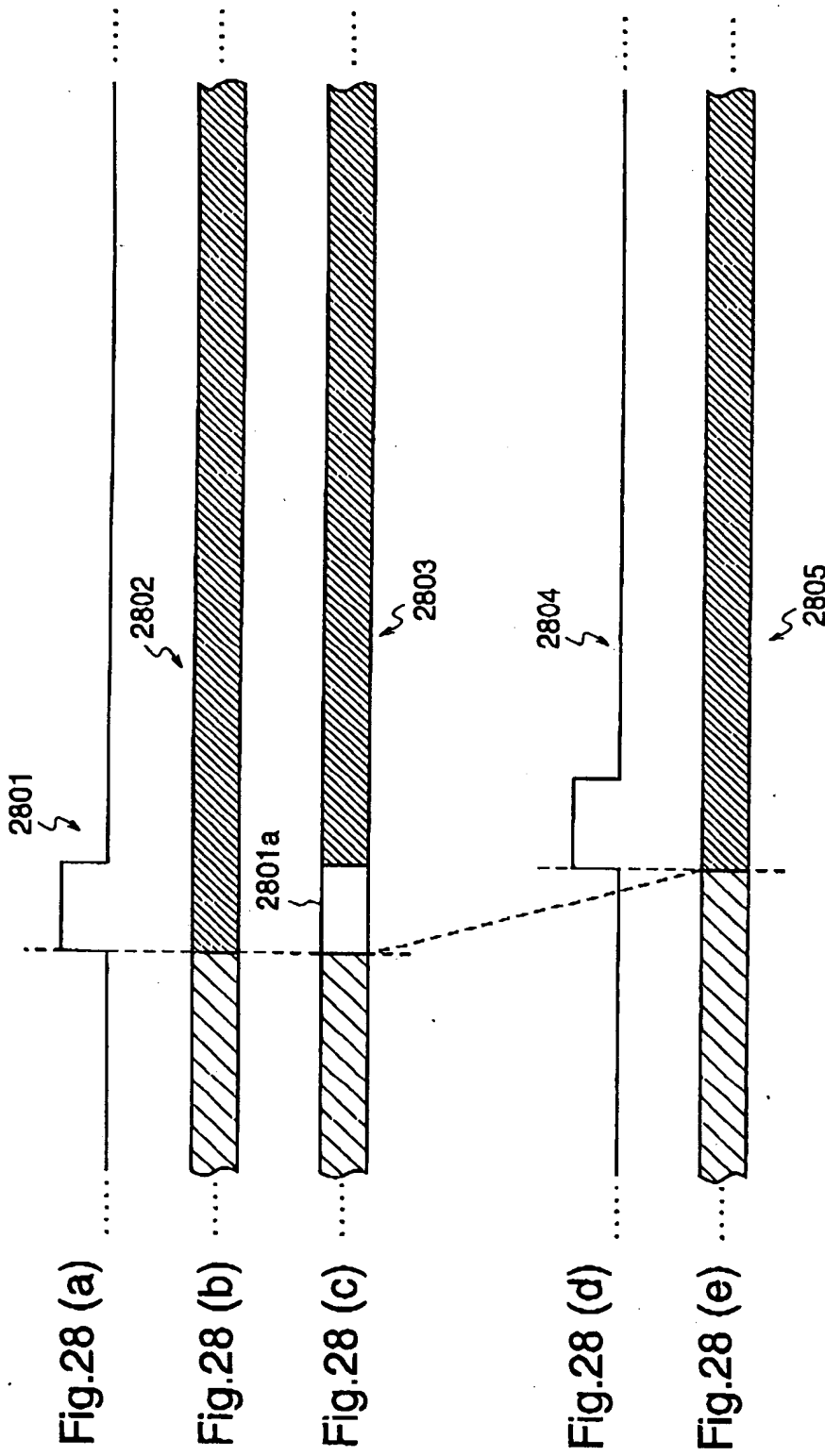


Fig.29 (a)

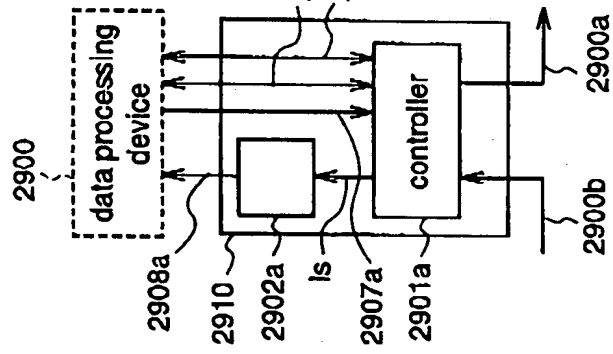


Fig.29 (b)

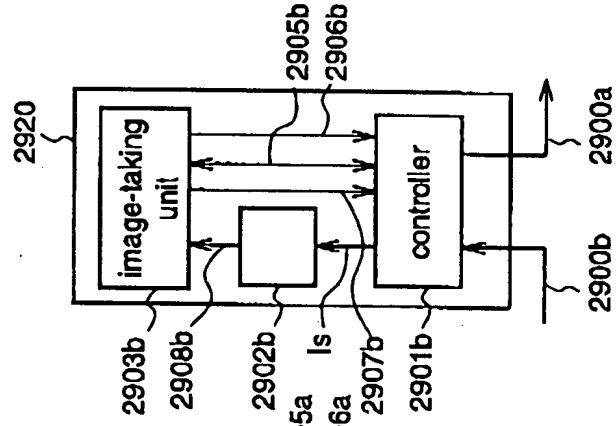


Fig.29 (c)

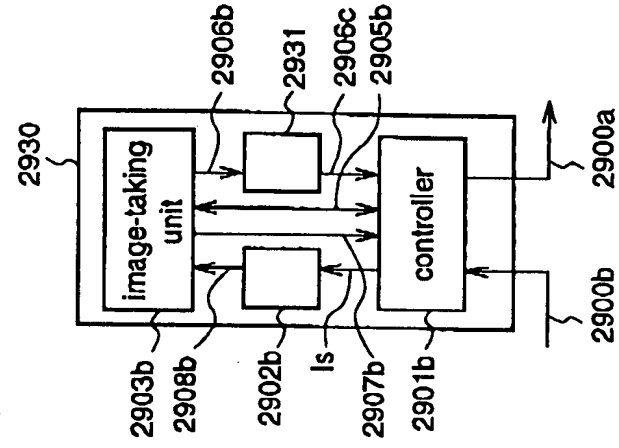


Fig.30 Prior Art

